REMARKS

In response to the Final Office Action dated December 12, 2006, claims 1 and 23 are amended. Claims 1-28 are now active in this application. No new matter has been added. The amendments are supported, at a minimum, by the specification at page 5, lines 15-17, and FIG. 1.

Claims 1-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Trimberger (U.S. Patent 5,737,631) in view of (U.S. Patent 5,136,697).

Independent claim 1 recites, in pertinent part, "a **dedicated control processing facility comprising a control execution path having its own control register file**; and a **dedicated data processing facility having its own data register file**, the data processing facility comprising a first data execution path including fixed operators and a second data execution path including at least configurable operators, said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction; wherein said decode unit is operable to detect whether a data processing instruction defines a fixed data processing operation or a configurable data processing operation, said decode unit causing the computer system to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected."

Specifically, FIG. 1 illustrates an embodiment of the claimed invention, wherein a computer processor has separate control and data processing facilities. In addition to having its own interface to the decode unit 101, the control processing unit 102 has its own control register file 104 and execution unit 107. Likewise, the data processing unit 103 has its own interface to the decode unit 101 as well as its own data register file 105, and both a fixed execution unit 109 and a configurable execution unit 110.

As stated at pages 7 and 8 of the present application, an instruction packet 100 supplied to the decode unit 101 can be one of three types:

1) Instruction packet 211 which contains only control instructions;

2) Instruction packet 212 which contains a data instruction and a memory instruction; and

3) Instruction packet 213, which contains a data instruction and a control instruction.

Accordingly, when a packet of type 211 is decoded all of the control instructions contained in the packet are sent to the control execution unit 102 for processing; when a packet of type 212 is decoded the data instruction and the memory instruction contained in the packet are sent to the data execution unit 103 for processing; and when a packet of type 213 is decoded the data instruction contained in the packet is sent to the data execution unit 103 for processing and the control instruction contained in the packet is sent to the control execution unit 102 for processing.

An important advantage of this arrangement is that when a first packet is a control packet of type 211, then the instructions are all sent to the control execution unit. Then when the next packet is a data packet of type 212 the instructions are all sent to the data execution unit for processing. These two packets can then be processed simultaneously, the control packet 211 in the control execution unit 102 and the data packet 212 in the data execution unit 103. This arrangement is advantageous over computer processors of the prior art in that the processing speed is greatly increased.

In order to establish *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. *In re Rokya*, 490 F. 2d 981, 180 USPQ

580 (CCPA 1974). At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitation.

Trimberger merely discloses a general-purpose processor having a fixed execution unit and a configurable execution unit. For example, Trimberger, at FIG. 2, item 100, merely discloses a data processing facility comprising a first data execution path including fixed operators. Thus, Trimberger does not benefit from the synergies of having dedicated control and data sides, with the data side comprising a fixed and a configurable data path, wherein the fixed and the configurable data paths may be considered as sub-paths of the data path. In addition, Trimberger uses the fixed execution unit for both control and data processing, and thus does not benefit from parallelism.

Thus, Trimberger does not teach or suggest a dedicated control processing facility comprising a control execution path having its own control register file; and a dedicated data processing facility having its own data register file.

Additionally, Johnson merely discloses a classic conventional super-scaler architecture including only one processing path. Therefore, if more than one instruction is issued at one time, then these instructions have to be ordered so that the computer processor does not try to execute these instructions using the same components at the same time, and so that there is no collision at any point in the hardware. This necessary ordering of the instructions slows the computer processor of Johnson when compared with the claimed invention.

Further, an essential feature of the structure of Johnson is the reorder buffer which is used to order the instructions. The computer processor of the present application does not require a reorder buffer. Therefore the structure of the claimed invention requires less power than Johnson.

Thus, Applicant respectfully submits that independent claim 1 is distinguished over the cited publications.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

Thus, it is respectfully submitted that dependent claims 2-21 are also allowable.

Applicant respectfully submit that independent claims 22-25 are distinguished over the cited publications for reasons similar to independent claim 1, as discussed above.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claim 25 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

Thus, it is respectfully submitted that dependent claims 26-28 are also allowable.

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Ed García-Otero

Eduardo Garcia-Otero
Registration No. 56,609

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 SAB/EG:cac
Facsimile: 202.756.8087
Date: May 14, 2007

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